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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,214	03/29/2002	Timothy S. Lehner	BUR920010175	7092

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EXAMINER	
PROCTOR, JASON SCOTT	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,214	LEHNER ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 were presented for examination. In response to a restriction requirement, Applicants have elected claims 1-10. Claims 1-10 have been rejected.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-10, drawn to a circuit model, classified in class 703, subclass 14.

II. Claims 11-22, drawn to a method of modeling an integrated circuit, classified in class 703, subclass 2.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case invention I, a circuit model, can be used with a different process of using. Invention II, a method of modeling a circuit, does not require the model defined by invention I. Both criteria for distinctness have been met, thus the restriction is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Richard Kotulak (27,712) on 18 August 2005 a provisional election was made without traverse to prosecute the invention of group I, claims 1-10. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

2. The disclosure is objected to because of the following informalities: There appear to be several spelling or grammatical errors in the specification. While the Examiner is aware that perfection is not required of the written description, in circumstances where Applicants' intended disclosure is unclear, corrections should be required.

In paragraph 0063, the phrase "self-consistently" is presumed to be "self-consistency". If this presumption is incorrect, the Examiner respectfully requests clarification.

Paragraphs 0065, 0068, and elsewhere make reference to "#5" or "#3", etc., the meaning of which is unknown. They do not appear to refer to, for example, equation 5 or equation 3. The Examiner is unaware of any other numbered concepts in the disclosure.

Paragraphs 0031 and 0032 depict equations, however the labels "Equation 2a" and "Equation 2b" are not separated from the equations by parenthesis, as has been done for other

equations (e.g. paragraph 0029). Consistency in the labeling of equations is required to clearly convey the equations used by Applicants.

Paragraph 0070 depicts an equation that appears to be missing a right parenthesis.

Applicants are respectfully encouraged to review the specification and to make amendments as necessary to ensure that the invention is clearly and accurately described.

Appropriate correction is required.

3. The use of the trademarks SPECCTRAQUEST™, XTK®, and CSE™ has been noted in this application. They should be capitalized wherever they appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claims 1 and 8 are directed toward "a circuit", however recite limitations such as "internal impedance, Zint, connected to the output node", "a Miller capacitor", or "an

ideal current source" (claim 8), all of which are not recognized as tangible real components of a circuit. For example, the term "Miller capacitor" apparently refers to a normal capacitor that models the well-known Miller effect. The term "Miller capacitor" is otherwise unknown in the art and does not refer to a particular type of capacitor. More to the point, impedance is a property of an electrical circuit, and is not a tangible component that can be literally connected to the output node. A circuit model, however, may contain intangible components that explain or account for the behavior and characteristics of a real circuit. These claims appear to be directed toward "a circuit model", not a circuit.

In summary, "a circuit" explicitly defined as including "a Miller capacitor", "internal impedance [...] connected to the output node", or "an ideal current source" cannot be regarded as an actual, tangible, real circuit. Applicants' limitations describe an abstract circuit model rather than an actual circuit. The Examiner respectfully suggests amending the preamble to recite "A circuit model" to address this indefiniteness under 35 U.S.C. § 112.

Claims 3 and 9 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 3 and 9 recite that components of the circuit model are "assumed" to be full functions of the input and output voltage, the meaning of which is unclear. The Examiner respectfully submits that it would be impossible to determine what assumptions were made by inventors of the prior art. This limitation fails to define the invention.

Claim 4 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner has presumed claim 4 contains two grammatical errors: a missing colon in "three elements: a near capacitor" and a superfluous concluding period. Correction is required. If these presumptions are incorrect, the meaning of claim 4 is unknown.

Claim 5 recites the limitations "the p transistor" and "the n transistor". There is insufficient antecedent basis for this limitation in the claim.

Claim 5 is further rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites "p transistor" and "n transistor", the meaning of which is unknown. The Examiner respectfully submits that terms such as "pnp transistor" are known in the art, but is unaware of an industry standard definition for "p transistor".

Claim 6 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 appears to contain grammatical errors that render the meaning of the claim unclear. Specifically, claim 6 does not contain a verb in the independent clause. It is therefore impossible to determine what Applicants' intended limitation might be and therefore will not be treated on the merits.

Claim 7 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites that "each current source could be [split] up" and thus fails to define the invention. The claim fails to recite a definite limitation of the invention, but instead suggests potential modifications to the claimed invention. Such a recitation does not define the invention and will not be treated on the merits.

Claims rejected but not specifically mentioned stand rejected by virtue of their dependence.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1-10 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Independent claims 1 and 8 are interpreted as being directed to a "circuit model" in order to resolve several rejections under 35 U.S.C. § 112, second paragraph, as set forth above. These interpretations are in keeping with what Applicants' have invented, as best understood by the Examiner. (See, for example, specification, paragraphs 0014, 0027). However, a circuit model is nonstatutory because it is not a specific machine or apparatus, but is instead an abstract, intangible description of a real circuit's behavior. As such, a circuit model itself is nonfunctional descriptive material. Please see MPEP 2106 (IV)(B)(1).

Whenever practicable, Examiners should indicate how rejections under 35 U.S.C. § 101 may be overcome and how problems may be resolved. The Examiner cannot make such an indication in this case because of the teachings of the disclosure and the entirety of the claims, both of which are clearly directed to an abstract circuit model.

To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over "Microelectronic Circuits, Second Edition" by Adel S. Sedra and Kenneth C. Smith (Sedra).

Regarding claims 1 and 8, Sedra discloses an equivalent circuit model for small signal operation of a MOSFET amplifier (page 350, Fig. 7.23) including the recited elements of independent claims 1 and 8. Implicit in Sedra's disclosure is the larger circuit which employs a MOSFET amplifier, and therefore the requisite circuit components as would be recognized by a person of ordinary skill in the art, such as the voltage rails, current sources, and ground rails.

Sedra further discloses *"the feedback capacitance C_{gd} will take part in a Miller effect, resulting in a high input capacitance in parallel with C_{gs}."* (page 351). Applicants' Fig. 2 renames this capacitor as Cm.

Claims 2 and 9 recite laws of nature and are therefore implicitly disclosed in the related prior art. Ohm's Law teaches that current source is a function of the related voltage.

Claim 3 recites an assumption which does not limit the invention. Were this claim rewritten to positively recite the limitation, however, it would recite a law of nature. The Miller effect explains that a capacitance is a function of the related input and output voltage.

Claims 4 and 10 recite an output load model which is known in the art as a pi model. Official notice is taken that it is well known in the related art to use a pi model to simulate a capacitive load.

Claim 5 appears to recite a use limitation ("the first current source *is used to represent* the p transistor", etc.) but does not provide further explanation. Sedra discloses a model for a MOSFET amplifier and therefore the implicit current sources are used to model a pnp and an npn transistor.

It would have been obvious to a person of ordinary skill in the art of electrical engineering, in combination with his own knowledge of electrical engineering, to use the circuit

model disclosed by Sedra in combination with well known laws of nature or well known circuit models to arrive at Applicants' claimed invention. Motivation to do so would be the nature of the problem at hand, such as the particular problem of modeling the Miller effect in a circuit such as a MOSFET amplifier.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892. In particular, US Patent No. 5,796,985 to O'Brien et al. discloses a method for incorporating a Miller compensation for modeling electrical circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Examiner
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